

On the Accuracy of Direct Extraction of the Heterojunction-Bipolar-Transistor Equivalent-Circuit Model Parameters C_π , C_{BC} , and R_E

Martin W. Dvorak, *Member, IEEE*, and Colombo R. Bolognesi, *Senior Member, IEEE*

Abstract—Several basic small-signal equivalent-circuit models for bipolar transistors lead to simple analytical expressions for the model parameters in terms of measured values. This paper investigates the accuracy of these expressions for real transistors by applying the direct extraction equations to more complicated small-signal models. The extraction of the base/collector capacitance, base/emitter capacitance, and emitter resistance are considered. Analytically derived trends are illustrated using measurements on small-area high-speed InP/GaAsSb/InP double heterojunction bipolar transistors.

Index Terms—Circuit modeling, heterojunction bipolar transistor (HBT), parameter extraction, small signal.

I. INTRODUCTION

IN THE high-frequency characterization of microwave transistors, small-signal models are often used to parametrize complicated behaviors with relatively simple equations. A small-signal model is preferably designed so that the model parameters represent something physical in the transistor. There are fundamental limitations in using lumped-element circuit models to describe physical structures such as a bipolar transistor, but such small-signal models can be remarkably effective at describing transistor behavior across a wide range of frequencies. As well, many model parameters may directly and unambiguously be correlated with physical quantities. This allows meaningful feedback between characterization/analysis and the design/fabrication of transistors. Indeed, there is much information one can obtain from small-signal parameters without obtaining the complete small-signal model for a transistor. The magnitude of a capacitance, for instance, tells us about device area and doping levels.

This paper examines methods used for the direct extraction of certain small-signal parameters: the base/collector capacitance,

base/emitter capacitance, and emitter resistance. These parameters can be extracted directly by manipulation of the basic small-signal model equations; a parameter can be expressed as a simple function of the Y - or Z -parameters. However, real transistors need to be described by more complicated models. By applying the simple direct extraction equations to more complicated small-signal models, the validity of these equations for real transistors can be investigated analytically. We reinforce these findings with experimental results on InP/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) fabricated and characterized at Simon Fraser University, Burnaby, BC, Canada [1].

Previous papers on bipolar transistor modeling discussed the frequency ranges of validity of various equations used in direct parameter extraction, and some have examined the sensitivity of extracted parameters to model inaccuracies. Pehlke and Pavlidis only considered the effects of external inductances on extracted base/collector capacitances [2]. The work by Spiegel *et al.* looked at extracted base/collector capacitances with the base/collector divided into an intrinsic and extrinsic region [3]. Li and Prasad performed direct parameter extraction by dividing up the frequency axis into a set of ranges, determined by characteristic delay times of the transistors [4]. They did not, however, look at the base/emitter capacitance, and the present work extends on theirs in examining the validity of approximations made for the determination of the emitter resistance and base/collector capacitance. Horng *et al.* studied and exploited the effects of emitter inductances on directly extracted parameters [5]. Ouslimani *et al.* follow the work of [4] and describe more sophisticated methods for direct parameter extraction, which prescribes frequency ranges of validity for the many required model equations [6]. In this paper, various alternatives for the direct extraction of the base/collector capacitance and external emitter resistance are compared and contrasted: manipulation of the basic model equations indicates that direct extraction from both Y - and Z -parameters is possible, and (in the simplest models) both give the same results.

In Section II, two well-known basic bipolar transistor models—the T -equivalent and hybrid- π models—are presented in a tutorial manner, and the effects of additional parameters on the model equations are examined. The direct extraction of the base/collector capacitance C_{BC} , base/emitter

Manuscript received April 15, 2002; revised November 25, 2002. This work was supported by the Natural Sciences and Engineering Research Council of Canada.

M. W. Dvorak was with the School of Engineering Science, Simon Fraser University, Burnaby, BC, Canada V5A 1S6. He is now with the Semiconductor Research and Development Division, Microwave Technology Center, Agilent Technologies, Santa Rosa, CA, 95403 USA.

C. R. Bolognesi is with the School of Engineering Science, Simon Fraser University, Burnaby, BC, Canada V5A 1S6.

Digital Object Identifier 10.1109/TMTT.2003.812557

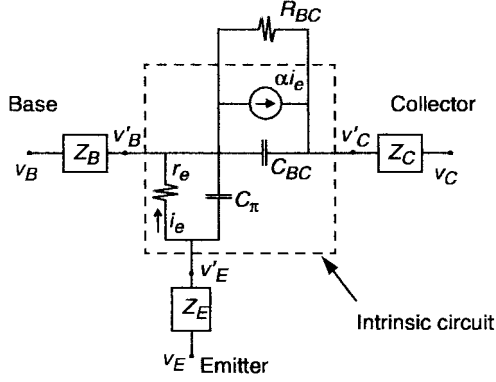


Fig. 1. Simplified T equivalent circuit for bipolar transistor. Intrinsic circuit is indicated inside the dashed box. External impedances are represented by Z_E , Z_B , and Z_C . Finite output impedance is represented by R_{BC} . Pad capacitances are not shown.

capacitance C_π , and emitter resistance $R_E + r_e$ using various techniques are then analyzed. A summary of findings concludes this paper.

II. BASIC MODEL EQUATIONS

In this section, two well-known basic bipolar transistor equivalent-circuit models are reviewed: the T -equivalent and hybrid- π circuit models. Circuit equations for these basic models are given, and some complications to the simple models are presented.

A. T Equivalent-Circuit Model

Fig. 1 shows the simplified T equivalent circuit for a bipolar transistor. The part inside the dashed box is the intrinsic simplified T equivalent-circuit model, and the impedances surrounding the intrinsic transistor (Z_E , Z_B , and Z_C) consist of a resistor and an inductor in series. The intrinsic Y' -parameters are

$$Y' = \begin{bmatrix} (1 - \alpha) \frac{1}{r_e} + j\omega(C_\pi + C_{BC}) & -j\omega C_{BC} \\ \frac{\alpha}{r_e} - j\omega C_{BC} & j\omega C_{BC} \end{bmatrix}. \quad (1)$$

For a compact Z -parameter representation, the current generator term is defined in terms of the total emitter current i_e entering the resistance r_e giving

$$Z' = \begin{bmatrix} Z_{BE} & Z_{BC} \\ Z_{BC} - \alpha_F Z_{BC} & Z_{BC} + (1 - \alpha_F) Z_{BC} \end{bmatrix} \quad (2)$$

where the impedances are $Z_{BC} = 1/(1/r_e + j\omega C_\pi)$ and $Z_{BE} = 1/j\omega C_{BC}$.

There is a subtle difference between the two approaches, as discussed in [8]. The transistor parameters α_F and α are related to the dc common base current gain α_0 , and include terms to account for various delay terms. The parameter α includes modifications to the magnitude and phase as functions of frequency as a consequence of the base/collector depletion layer transit times giving

$$\alpha = \alpha_0 \left[\frac{\sin(\omega\tau_C)}{\omega\tau_C} \right] \exp(-j\omega\tau) \quad (3)$$

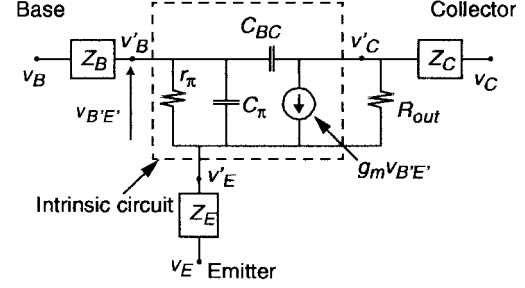


Fig. 2. Simplified hybrid- π equivalent circuit for bipolar transistor. The intrinsic circuit is indicated inside the dashed box. External impedances (a resistor and inductor in series) are represented by Z_E , Z_B , and Z_C . Finite output impedance is represented by R_{out} . Pad capacitances are not shown.

where τ_C is the collector transit time and τ is an empirical delay time consisting of the collector transit time and a small portion of the base transit time. However, the base/emitter delay is absorbed by the base/emitter RC circuit. In contrast, the parameter α_F , which is used in the Z -parameter version of the T equivalent circuit, does include the base/emitter delay. It is given by [8]

$$\alpha_F = \frac{\alpha}{1 + \frac{j\omega}{\omega_B}} \quad (4)$$

where ω_B represents an additional first-order magnitude and phase shift caused by the base/emitter delay. This latter is used in the Z -parameter version of the small-signal model.

B. Hybrid- π Equivalent-Circuit Model

Fig. 2 shows the simplified T equivalent circuit for a bipolar transistor. The intrinsic Y' -parameters for this two port can be shown to be

$$Y' = \begin{bmatrix} \frac{1}{r_\pi} + j\omega(C_\pi + C_{BC}) & -j\omega C_{BC} \\ g_m - j\omega C_{BC} & j\omega C_{BC} \end{bmatrix}. \quad (5)$$

Note that the hybrid- π and T equivalent model equations are identical if the following substitutions are made:

$$r_\pi = \frac{r_e}{1 - \alpha} \text{ and } g_m = \frac{\alpha}{r_e}. \quad (6)$$

Otherwise, all parameters are equivalent, and notably the base/emitter and base/collector capacitances are unchanged. Extrinsic parameters are also unchanged.

C. Finite Output Impedance

The output impedance is added in one of two ways. It may be added as a conductance between the base and collector, as is usually the case for T equivalent circuits (Fig. 1). In this case, the effects of the output conductance are added by replacing each instance of $j\omega C_{BC}$ with $j\omega C_{BC} + 1/R_{BC}$.

Or it is added as a conductance between the emitter and collector, as is usually drawn for hybrid- π equivalent circuits (Fig. 2). In this second case, the output conductance is added as an admittance to the intrinsic Y -parameters

$$Y' = \begin{bmatrix} Y'_{11} & Y'_{12} \\ Y'_{21} & Y'_{22} + \frac{1}{R_{out}} \end{bmatrix}. \quad (7)$$

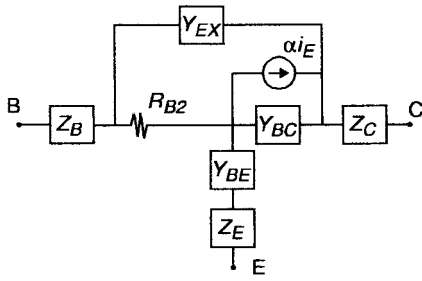


Fig. 3. Wei and Hwang's full T equivalent circuit for bipolar transistor [10]. External capacitances are not shown.

D. Extrinsic/Intrinsic Base/Collector Capacitance:

Y -Parameters

More accurate bipolar transistor models must take into account the extrinsic and intrinsic components of the base/collector capacitance, which are separated by an internal base resistance; this distributed nature of the base/collector junction is very important in estimating the f_{MAX} of a heterojunction bipolar transistor (HBT) [9]. A T equivalent circuit with this modification is shown in Fig. 3. The model equations in terms of the simplified intrinsic Y -parameters (not including external impedances) are

$$\begin{aligned} Y_{11} &= \frac{Y'_{11}}{R_{B2}Y'_{11} + 1} + j\omega C_{EX} \\ Y_{12} &= \frac{Y'_{12}}{R_{B2}Y'_{11} + 1} + j\omega C_{EX}. \end{aligned} \quad (8)$$

Resistances in parallel with C_{EX} are not included in the above expressions.

E. Extrinsic/Intrinsic Base/Collector Capacitance:

Z -Parameter Expressions

For some calculations it is more convenient to use Z -parameter expressions for the T equivalent-circuit model including the effects of the distributed base/collector junction. Wei and Hwang [10] used the equivalent-circuit model of Fig. 3, which conveniently includes the parasitic series inductances Z_B , Z_E , and Z_C . Note that to allow for a resistance in parallel with C_{BC} and C_{EX} , these terms are written as generic admittances Y_{BC} and Y_{EX} . Wei and Hwang provide the following model equations:

$$\begin{aligned} Z_{11} &= \frac{[(1 - \alpha_F)Z_{BC} + Z_{EX}]R_{B2}}{Z_{BC} + Z_{EX} + R_{B2}} + Z_{BE} + Z_B + R_E \\ Z_{12} &= \frac{(1 - \alpha_F)Z_{BC}R_{B2}}{Z_{BC} + Z_{EX} + R_{B2}} + Z_{BE} + Z_E \\ Z_{21} &= \frac{[-\alpha_F Z_{EX} + (1 - \alpha_F)R_{B2}]Z_{BC}}{Z_{BC} + Z_{EX} + R_{B2}} + Z_{BE} + Z_E \\ Z_{22} &= \frac{(1 - \alpha_F)Z_{BC} + (Z_{EX} + R_{B2})}{Z_{BC} + Z_{EX} + R_{B2}} + Z_{BE} + Z_C + Z_E. \end{aligned} \quad (9)$$

(Note that the current generator refers to the terminal emitter current, hence, the use of α_F instead of α .)

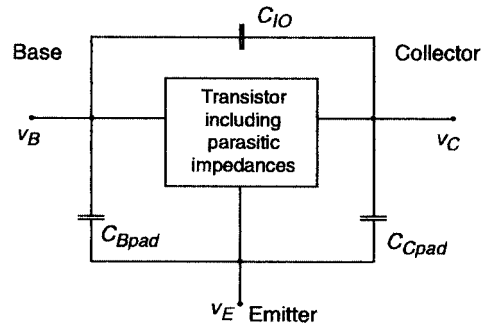


Fig. 4. Schematic showing placement of external parasitic capacitances: C_{Bpad} is the base pad capacitance, C_{Cpad} is the collector pad capacitance, and C_{IO} is the input/output capacitance.

F. Adding External Capacitances and Impedances

To add external impedances to any of the above circuits, the impedances (shown in Fig. 1) are added to the Z -parameters in series as follows:

$$Z = \begin{bmatrix} Z'_{11} + Z_B + Z_E & Z'_{12} + Z_E \\ Z'_{21} + Z_E & Z'_{22} + Z_C + Z_E \end{bmatrix} \quad (10)$$

where $Z_i = R_i + j\omega L_i$ for each of the emitter, base, and collector terminals. When deembedding of parasitics is performed, the pad inductances should be removed almost entirely, but some external series resistances will remain because ohmic contacts are generally considered to be part of the complete transistor.

The pad capacitances, shown in the small-signal equivalent-circuit model in Fig. 4, are added using Y -parameters [11]. The Z -parameters of the intrinsic device with external impedances are converted to Y -parameters, and then the following calculation is made:

$$\begin{aligned} Y &= Y' + Y_{pad} \\ &= \begin{bmatrix} Y'_{11} + Y_{Bpad} + Y_{IO} & Y'_{12} - Y_{IO} \\ Y'_{21} - Y_{IO} & Y'_{22} + Y_{Cpad} + Y_{IO} \end{bmatrix} \end{aligned} \quad (11)$$

where $Y_i = j\omega C_i$ for each of the capacitive admittances.

In this study, the external pad impedances, inductances, and capacitances have been removed by the inverse procedure, with capacitances and impedances having been determined from dummy OPEN and SHORT pads. However, some residual parasitics from imperfect deembedding always remain. Generally, inductances for larger devices and capacitances for smaller devices are the important parasitic elements at high frequencies.

III. BASE/COLLECTOR CAPACITANCE EXTRACTION

A. From Basic Model Equations

A base/collector capacitance may be extracted using the T equivalent-circuit Z -parameter relations in (2) as follows:

$$\tilde{C}_{BC}(Z) \equiv \frac{1}{\omega \text{Im}\{Z_{22} - Z_{21}\}}. \quad (12)$$

(This is identically equivalent to the H -parameter expression for base-collector capacitance used in [2].) As will be shown later, a better approach is to take the imaginary part of the admittance instead [12] as follows:

$$C_{BC}(Z) \equiv \text{Im} \left\{ \frac{1}{\omega \{Z_{22} - Z_{21}\}} \right\}. \quad (13)$$

Based on the simplified equivalent-circuit models, the same value for base/collector capacitance $C_{BC}(Y)$ appears to be extracted using Y -parameters using the relation in (1) as follows:

$$C_{BC}(Y) \equiv \frac{\text{Im}\{Y_{12}\}}{\omega}. \quad (14)$$

However, inaccuracy can result from the use of $C_{BC}(Y)$ when the effect of extrinsic/intrinsic base/collector capacitance is included. By putting (1) into (8), we obtain for Y_{12}

$$Y_{12} = \frac{-j\omega C_{BC}}{R_{B2} \left((1-\alpha) \frac{1}{r_e} + j\omega (C_\pi + C_{BC}) \right) + 1} - j\omega C_{EX}. \quad (15)$$

The base/emitter capacitance and base/collector capacitance in the denominator are ignored (since $\omega R_{B2}(C_\pi + C_{BC}) \ll 1$ at our measurement frequencies), thus,

$$C_{BC}(Y) \approx \frac{C_{BC}}{(1-\alpha) \frac{R_{B2}}{r_e} + 1} + C_{EX}. \quad (16)$$

For larger devices, r_e is small (order of 1Ω), and R_{B2} can be substantial (tens of ohms). For a typical β (approximately 50) giving $(1-\alpha) \sim 0.02$, the denominator in the first term may not be that close to unity. This technique, therefore, fails under not too uncommon circumstances.

When a transistor is in forward active operation (typical for high-frequency characterization), the Y -parameter technique may, therefore, lead to inaccuracies. Potentially, in a transistor with sufficiently low dc gain and large ratios between the base and emitter resistances, the different values obtained $C_{BC}(Y)$ and $C_{BC}(Z)$ may be used to help separate the intrinsic and extrinsic base/collector capacitance components.

On the other hand, when a transistor is “cold”—very weakly forward active biased (at or below the base/emitter turn-on voltage) or in cutoff (both base/collector and base/emitter junctions reverse biased)—then the current gain α may be very small, hence, $(1-\alpha) \sim 1$, but r_e will be very large. Thus, the denominator in (16) will go to unity as follows:

$$C_{BC}(Y) \approx C_{BC} + C_{EX}. \quad (17)$$

Thus, $C_{BC}(Y)$ is accurate even for larger emitter transistors when they are under “cold” bias or in cutoff.

The base/collector capacitance $C_{BC}(Z)$ extracted from Z -parameters, in contrast, is well behaved in transistors under forward active operation [3]. From Wei and Hwang’s expression for the model Z -parameters in (9) (neglecting external impedances)

$$\begin{aligned} \frac{1}{Z_{22} - Z_{21}} &\approx \frac{Z_{BC} + Z_{EX} + R_{B2}}{Z_{BC} Z_{EX}} \\ &= Y_{BC} + Y_{EX} + \frac{R_{B2}}{\frac{1}{Y_{BC}} \frac{1}{Y_{EX}}} \\ \therefore C_{BC}(Z) &\equiv \text{Im} \left\{ \frac{1}{\omega \{Z_{22} - Z_{21}\}} \right\} = C_{BC} + C_{EX}. \end{aligned} \quad (18)$$

Therefore, the extracted base/collector capacitance equals the sum of the intrinsic and extrinsic capacitances. Comparisons of the Y -parameter-extraction technique to the Z -parameter technique are shown in Fig. 5 for a narrow emitter stripe and Fig. 6

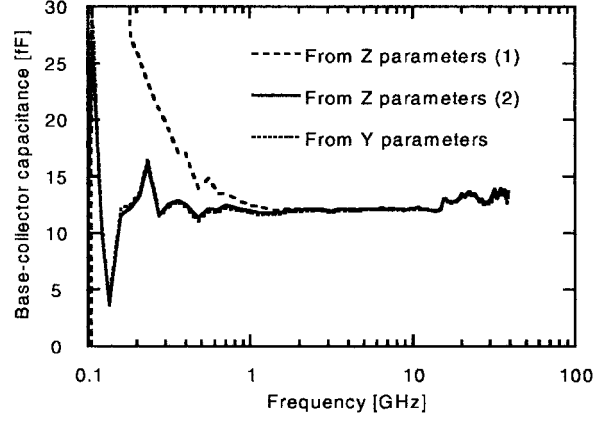


Fig. 5. Comparison of extracted base/collector capacitance of $0.5 \times 12 \mu\text{m}^2$ emitter metal device using three different extraction techniques: (dashed line) from Z -parameters using (12); (solid line) from Z -parameters using (13); (dotted line) from Y -parameters using (14). The values for the two latter techniques are nearly identical for this device. The increased apparent capacitance when using (12) results from the finite output impedance.

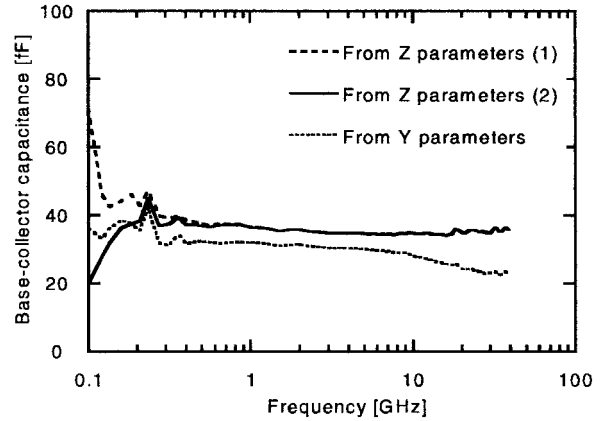


Fig. 6. Comparison of extracted base/collector capacitance of $2.0 \times 24 \mu\text{m}^2$ emitter metal device using three different extraction techniques: (dashed line) from Z -parameters using (12); (solid line) from Z -parameters using (13); (dotted line) and from Y -parameters using (14). The reduced value of base capacitance obtained from Y -parameters is because of the large R_{B2} related to spreading resistance under the emitter. Also, the bias current is large so r_e is small. Compare with Fig. 5, which is for a device fabricated simultaneously, but with a narrower emitter.

for a wider emitter stripe. When the base spreading resistance is large and the emitter resistance is small, then the R_{B2} term causes $C_{BC}(Y)$ to drop from the limiting value of $C_{BC} + C_{EX}$.

B. Effects of Pad Capacitances

The input pad capacitance C_{Bpad} does not affect $C_{BC}(Z)$ because $C_{BC}(Z)$ is derived from the output Z -parameters Z_{22} and Z_{21} . An input/output capacitance will add to $C_{BC}(Z)$ in the same way that the intrinsic/extrinsic parts of the base/collector capacitance add. The effect of the output pad capacitance is more interesting. For the circuit shown in Fig. 4, with $C_{Bpad} = 0$ and $C_{IO} = 0$, the extrinsic Z_{21} and Z_{22} in terms of intrinsic Z' -parameters Z' become

$$\begin{aligned} Z_{21} &= Z'_{21} \left(1 - \frac{Z'_{22}}{Z'_{22} + Z_p} \right) \\ Z_{22} &= \frac{Z_p Z'_{22}}{Z'_{22} + Z_p} \end{aligned} \quad (19)$$

where we define $Z_p = 1/j\omega C_{\text{pad}}$. The Z -parameters of the intrinsic circuit are assumed to be

$$Z' = \begin{bmatrix} Z_{\text{BE}} & Z_{\text{BE}} \\ Z_{\text{BE}} - \alpha_F Z_{\text{BC}} & Z_{\text{BE}} - (1 - \alpha) Z_{\text{BC}} \end{bmatrix} \quad (20)$$

for simplicity. C_{BC} is calculated using (19) and (20) as follows:

$$\frac{1}{Z_{22} + Z_{21}} = \frac{Z_{\text{BE}} - (1 - \alpha_F) Z_{\text{BC}} + Z_p}{Z_p Z_{\text{BC}}}. \quad (21)$$

In transistors under forward active bias, Z_{BE} may be ignored because it is much smaller than the other two impedances. After substituting for the definitions of Z_{BC} and Z_p , and using (13) to find $C_{\text{BC}}(Z)$, this becomes

$$\begin{aligned} \frac{1}{Z_{22} - Z_{21}} &\approx (1 - \alpha_F) j\omega C_{\text{pad}} + j\omega C_{\text{BC}} \\ \therefore C_{\text{BC}}(Z) &\equiv \text{Im} \left\{ \frac{1}{\omega \{Z_{22} - Z_{21}\}} \right\} \approx (1 - \alpha_0) C_{\text{pad}} + C_{\text{BC}}. \end{aligned} \quad (22)$$

Therefore, the extracted base/collector capacitance $C_{\text{BC}}(Z)$ will include a contribution from the collector pad capacitance. As long as the current gain is high, then this contribution should not be important, except on very small devices. For 2000-Å collectors, the base/collector capacitance is approximately 0.5 fF/ μm^2 , whereas the error in pad deembedding should not exceed more than a few femtofarads. To put in some numbers in a realistic “worst-case” example, let us assume a deembedding error of 2 fF, a gain of ten, and a base–collector area of 2 μm^2 (i.e., $C_{\text{BC}} \sim 1$ fF). The deembedding error will then be 0.2 fF or 20%.

The assumption made in (22) (that Z_{BE} is small) no longer holds for devices under “cold” bias. Under such conditions, the dynamic emitter resistance r_e is very large and the extracted base/collector capacitance will instead be

$$\begin{aligned} \frac{1}{Z_{22} - Z_{21}} &= \frac{1}{Y_{\text{BE}} + \frac{(1 - \alpha_F)}{Y_{\text{BC}}} + \frac{1}{Y_p}} \\ &= \frac{Y_p Y_{\text{BC}}}{Y_p Y_{\text{BC}} + (1 - \alpha_F) Y_p + Y_{\text{BC}}} \\ &= \left(\frac{C_{\text{BC}}}{C_\pi} \right) j\omega C_{\text{pad}} + (1 - \alpha_F) j\omega C_{\text{pad}} \\ &\quad + j\omega C_{\text{BC}} \\ \therefore C_{\text{BC}}(Z) &\equiv \text{Im} \left\{ \frac{1}{\omega \{Z_{22} - Z_{21}\}} \right\} \\ &\approx \left(\frac{C_{\text{BC}}}{C_\pi} \right) C_{\text{pad}} + (1 - \alpha_F) C_{\text{pad}} + C_{\text{BC}}. \end{aligned} \quad (23)$$

Thus, the contribution from the collector pad capacitance will be multiplied by the ratio of the base/collector and base/emitter capacitances. In our devices, the ratio between these junction capacitances typically ranges from about unity for 2- μm emitter devices to as high as ten for submicrometer emitter devices (C_π is small in “cold” bias). Since the collector pad capacitance is on

the order of tens of femtofarads, an error of a few femtofarads is to be expected from deembedding. Small-emitter devices under “cold” bias may, therefore, have very large percentage errors in $C_{\text{BC}}(Z)$ associated with inaccurate deembedding of C_{pad} .

The extracted base/collector capacitance $C_{\text{BC}}(Y)$ is sensitive only to the base/collector pad capacitance C_{TO} since it is obtained from Y_{12} [see (11)].

C. Effects of Finite Output Impedance

There are several effects on the extracted base/collector capacitance $C_{\text{BC}}(Z)$ when there is finite output impedance. First, the effect of an output conductance in parallel with the base/collector capacitance (Fig. 1) is considered. If C_{BC} is extracted using the formula for $C_{\text{BC}}(Z)$ in (12) then, at low frequencies, C_{BC} will include a contribution from the finite real output conductance because it is acting in parallel to the base/collector capacitance $j\omega C_{\text{BC}} \Rightarrow j\omega C_{\text{BC}} + G_{\text{BC}}$. The characteristic frequency below which this effect appears is $1/2\pi f \approx R_{\text{BC}} C_{\text{BC}}$, which is typically below 1 GHz. If, however, the formula of (13) is used, i.e., the capacitance is assumed to be parallel to a conductance and, thus, it forms the imaginary part of an *admittance*, then this effect disappears entirely. Fig. 5 shows the improved behavior at low frequencies when using (13) instead of (12).

However, an output conductance parallel with the intrinsic base/collector capacitance may act to increase the extracted capacitance [12], [13]

$$\begin{aligned} C_{\text{BC}}(Z) &\equiv \text{Im} \left\{ \frac{1}{\omega \{Z_{22} - Z_{21}\}} \right\} \\ &= C_{\text{BC}} + C_{\text{EX}} (1 + R_{B2} G_{\text{BC}}). \end{aligned} \quad (24)$$

For our DHBTs, the $R_{B2} G_{\text{BC}}$ is much smaller than unity and this effect can be ignored.

The finite output impedance interacting with the collector pad capacitance may cause a similar problem. By taking (22) and replacing the collector pad admittance with the output admittance $1/R_{\text{out}}$ (compare Figs. 2 and 4), the extracted $C_{\text{BC}}(Z)$ becomes

$$\begin{aligned} \frac{1}{Z_{22} - Z_{21}} &= \frac{1 - \alpha_F}{R_{\text{out}}} + j\omega C_{\text{BC}} \\ &\approx \frac{1 - \alpha_0 (1 - j\omega \tau_d)}{R_{\text{out}}} + j\omega C_{\text{BC}} \\ \therefore C_{\text{BC}}(Z) &= \frac{\alpha_0 \tau_d}{R_{\text{out}}} + C_{\text{BC}} + \text{imaginary term}. \end{aligned} \quad (25)$$

For simplicity, the first-order behavior of α_F is modeled using a single time constant τ_d . The extracted base/collector capacitance is increased because of the additional first term. Fortunately, R_{out} is very large (kilohms) and τ_d is very small (< picosecond) and, thus, the additional term is negligible in our devices.

D. Effects of Parasitic Impedances on $C_{\text{BC}}(Z)$

From the Z -parameters expressions (9) and the definition for $C_{\text{BC}}(Z)$ in (12), only the collector impedance should affect the extracted C_{BC} as follows:

$$C_{\text{BC}}(Z) = \frac{C_{\text{BC}}}{1 - \omega^2 L_C C_{\text{BC}}}. \quad (26)$$

At higher frequencies, the extracted base/collector capacitance, therefore, increases. If the expression (13) for $C_{BC}(Z)$ is used instead, then

$$C_{BC}(Z) = C_{BC} \times \frac{(1 - \omega^2 L_C C_{BC})}{(1 - \omega^2 L_C C_{BC})^2 + (\omega R_C C_{BC})^2}. \quad (27)$$

The terms $\omega^2 L_C C_{BC}$ and $(\omega R_C C_{BC})^2$ are both small for typical high-speed devices, thus, the external impedances should not affect the apparent $C_{BC}(Z)$.

IV. BASE/EMITTER CAPACITANCE EXTRACTION

A. Introduction

While there have been published attempts to obtain the base/emitter capacitance C_π by complicated manipulations (Li and Prasad [4] and Wei and Hwang [10]), others such as Spiegel *et al.* [3] and Pehlke and Pavlidis [2] state that this capacitance cannot be directly extracted from measured S -parameters. On the other hand, Chang *et al.* state that the base/emitter capacitance is directly determined from the input admittance when the base/collector and input pad capacitances are known [14]. These discrepancies may arise because the α term and the capacitance C_π cannot be obtained independently. To complicate matters, the capacitance C_π necessarily consists of a depletion capacitance depending on the base/emitter voltage, and a diffusion capacitance proportional to the collector current.

That is not to say that it is impossible to estimate the base/emitter capacitance from S -parameters. The base/emitter capacitance $C_\pi(Y)$ appears in the basic equations in (1) and, thus,

$$C_\pi(Y) \equiv \frac{1}{\omega} \text{Im} \{Y_{11} + Y_{12}\} = \frac{1}{\omega} \text{Im} \left\{ \frac{1}{r_\pi} + j\omega C_\pi \right\}. \quad (28)$$

This appears to give the final answer. Unfortunately, r_π is complex. It is defined by $r_\pi = r_e / (1 - \alpha)$. Since α is complex, the imaginary part of $Y_{11} + Y_{12}$ must include a contribution from r_π . Rewriting the above (assuming small $\omega\tau$, hence, taking first-order approximations throughout)

$$\begin{aligned} C_\pi(Y) &= \frac{1}{\omega} \text{Im} \left\{ \frac{1 - \alpha}{r_e} + j\omega C_\pi \right\} \\ &\approx \frac{1}{\omega} \text{Im} \left\{ \frac{1 - \alpha_0(1 - j\omega\tau)}{r_e} + j\omega C_\pi \right\} \\ &= \frac{\alpha_0\tau}{r_e} + C_\pi \approx \frac{\alpha_0\tau I_C}{n_C kT} + C_\pi. \end{aligned} \quad (29)$$

A typical delay time τ at normal biases will consist of the collector transit time and a small fraction of the base transit time, for a total of around 0.1 or 0.2 ps in the present devices (judging from minimum delay time measurements [1]). For a typical $1 \times 12 \mu\text{m}^2$ emitter area DHBT, at a bias of 24 mA, and, thus, $r_e \sim 1 \Omega$. The first term, therefore, will be on the order of ~ 100 fF, which is comparable to the typical C_π of 150 fF measured on a DHBT.

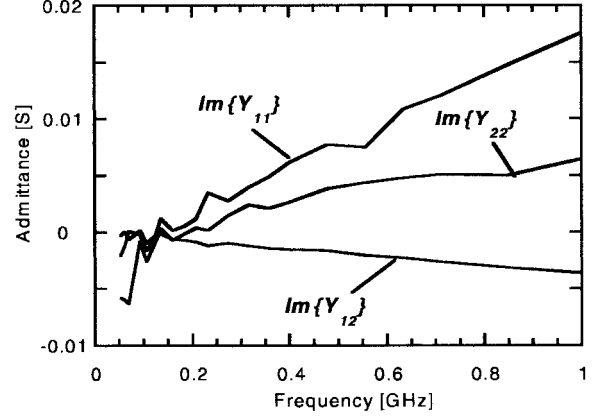


Fig. 7. Imaginary part of measured admittances Y_{11} , Y_{12} , and Y_{22} of device describe in Fig. 8. The admittances appear to have a zero intercept around 150 MHz. This is probably an artifact of imperfect calibration.

B. Distributed Base/Collector Effects

The above derivation used a simplified small-signal model. More accurate representations of the base/emitter capacitance $C_\pi(Y)$ are obtained by beginning with (8), i.e., with the distributed base/collector taken into account, and putting in the intrinsic Y -parameters from (1)

$$Y_{11} + Y_{12} = \frac{\frac{1}{r_\pi} + j\omega C_\pi}{R_{B2} \left(\frac{1}{r_\pi} + j\omega (C_\pi + C_{BC}) \right) + 1}. \quad (30)$$

This is expressed in terms of the previous result (28)

$$C_\pi(Y) = \frac{1}{\omega} \text{Im} \left\{ \left(\frac{1}{r_\pi} + j\omega C_\pi \right) \cdot \left(1 - \frac{\left(R_{B2} \left(\frac{1}{r_\pi} + j\omega (C_\pi + C_{BC}) \right) \right)}{1 + R_{B2} \left(\frac{1}{r_\pi} + j\omega (C_\pi + C_{BC}) \right)} \right) \right\}. \quad (31)$$

What is the significance of the correction term? When R_{B2} is small, then the correction term goes to unity (the trivial case). As R_{B2} increases, both the frequency-dependent and frequency-independent parts of the correction term will tend to reduce the apparent $C_\pi(Y)$. The correction term may be substantial. For example, for a relatively large device, at 30 GHz, with $R_{B2} \sim 10 \Omega$ and $C_\pi \sim 500$ fF, $\omega R_{B2} C_\pi \sim 1$. At low frequencies, the expression reduces to

$$C_\pi(Y) = \frac{1}{\omega} \text{Im} \left\{ \left(\frac{1}{r_\pi} + j\omega C_\pi \right) \left(1 - \frac{R_{B2}(1 - \alpha)}{r_e + R_{B2}(1 - \alpha)} \right) \right\}. \quad (32)$$

For typical high-speed devices, with $\alpha \sim 0.98$, $r_e \sim 1 \Omega$, and $R_{B2} \sim 5 \Omega$, the apparent $C_\pi(Y)$ will be reduced by the correction term by approximately 10%. Fig. 7 shows that, for wide

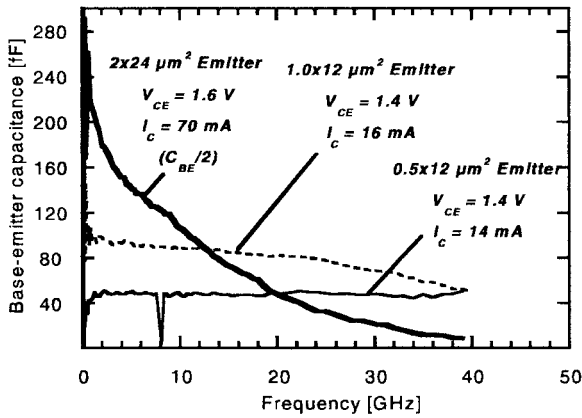


Fig. 8. Comparison of extracted base/emitter capacitance at similar current densities with identical base contact resistances, but different emitter finger widths (dimensions are nominal). Large emitter widths (i.e., large base spreading resistance devices) have poorly behaved extracted base/emitter capacitances. For the 2- μm emitter device, the capacitance divided by two is plotted.

emitter fingers, the extracted capacitance is a strong function of frequency, while for narrow emitters, it remains essentially constant across the measured frequency range. This is because devices with wide emitter fingers will have larger internal base resistances R_{B2} than ones with narrow emitters.

C. Output Conductance and Pad Capacitance Effects

What happens with even more complicated models? An output conductance parallel to the base/collector capacitance (i.e., each instance of $j\omega C_{BC}$ is replaced by $j\omega C_{BC} + 1/R_{BC}$) will not affect the extracted $C_\pi(Y)$ when using the simplest model and, in the more complicated model of (31), the resistance R_{BC} is so much larger than r_π that it can be ignored. A conductance across the collector/emitter terminals will have no effect since it only modifies Y_{22} . If the external pad capacitances are not removed, then $C_\pi(Y)$ will include the base pad capacitance; thus, pad deembedding is a source of error in extraction of $C_\pi(Y)$.

D. Other Effects

At very low frequencies (< 1 GHz), the extracted base/emitter capacitance has been observed to decrease dramatically (see the curve for the 0.5- μm emitter device in Fig. 7). This effect is not accounted for in the above discussion. A likely cause is the inaccuracies in the test set and/or calibration. The plots of $\text{Im}\{Y_{11}\}$, $\text{Im}\{Y_{12}\}$, and $\text{Im}\{Y_{21}\}$ in Fig. 8 show that they are straight lines with frequency axis intercepts at frequencies of approximately 150 MHz. This behavior cannot be described by a simple lumped-element equivalent-circuit model. Our test set (HP8516A) measures from 45 MHz to 40 GHz, and it is not unreasonable to assume that, at edges of the measurement range, the measurements may be less accurate. Therefore, other extracted parameters may also be inaccurate at very low frequencies (< 1 GHz).

V. EMITTER RESISTANCE EXTRACTION

The emitter resistance is an important parameter of the HBT because it can be responsible for a significant portion of the total emitter/collector delay time

$$\frac{1}{2\pi f_T} = r_e (C_{jBE} + C_{BC}) + (R_E + R_C) C_{BC} + \tau_B + \tau_C. \quad (33)$$

Here, the dynamic emitter resistance is given by $r_e = nkT/qI_C$, and R_E is the external series resistance (mostly the contact resistance) of the emitter. At peak cutoff frequencies for highly scaled HBTs, the dynamic resistance r_e can easily be responsible for a third of the delay time through emitter and collector charging times, while R_E is much larger than R_C and is responsible for most of the C_{BC} charging time.

A. From Z-Parameters

The emitter resistance $r_e + R_E$ can be found by taking the real part of Z_{12} . The first-order approximation for α_F is

$$\alpha_F = \frac{\alpha_0 \left[\frac{\sin(\omega\tau_C)}{\omega\tau_C} \right] \exp(-j\omega\tau)}{1 + j\frac{\omega}{\omega_B}} \approx \alpha_0 (1 - j\omega\tau') \quad (34)$$

where τ' is an effective first-order time constant and, thus, the real part of Z_{12} gives

$$\begin{aligned} \text{Re}\{Z_{12}\} &= \text{Re} \left\{ \frac{(1 - \alpha_F) Z_{BC} R_{B2}}{Z_{BC} + Z_{EX} + R_{B2}} + Z_{BE} + Z_E \right\} \\ &\approx \Delta + \frac{r_e}{1 + (\omega r_e C_\pi)^2} + R_E \end{aligned} \quad (35)$$

where

$$\Delta = \text{Re} \left\{ \frac{(1 - \alpha_0 (1 - j\omega\tau')) \frac{R_{B2}}{\frac{1}{R_{BC}} + j\omega C_{BC}}}{\frac{1}{\frac{1}{R_{BC}} + j\omega C_{BC}} + \frac{1}{j\omega C_{EX}} + R_{B2}}} \right\}.$$

The two right-hand terms will reduce to $r_e + R_E$ at normal measurement frequencies because the time $r_e C_\pi$ constant will normally be on the order of tens to a few hundreds of femtoseconds. At very low frequencies, when the $j\omega R_{BC}(C_{EX} + C_{BC})$ term is small compared to unity, the correction term Δ becomes

$$\Delta \approx \text{Re} \left\{ \frac{(1 - \alpha_0 (1 - j\omega\tau')) j\omega C_{EX} R_{B2} R_{BC}}{1 + j\omega R_{BC} (C_{EX} + C_{BC})} \right\} \quad (36)$$

which reduces to zero to first order. At moderate frequencies, when the $j\omega R_{BC}(C_{EX} + C_{BC})$ term is large compared to unity, the term becomes

$$\Delta \approx \frac{(1 - \alpha_0) C_{EX} R_{B2}}{C_{EX} + C_{BC}}. \quad (37)$$

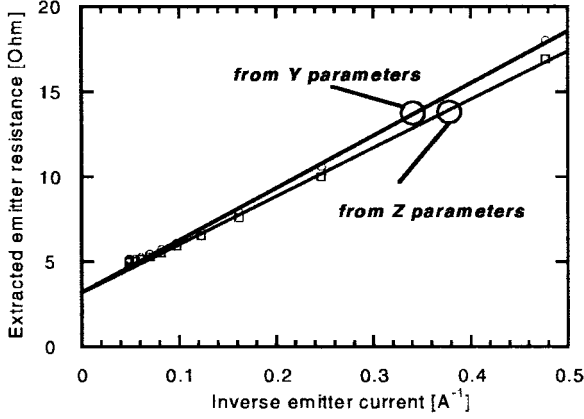


Fig. 9. Emitter resistances obtained either from the Z -parameter method (squares) or the Y -parameter method (circles). Lines are least-square fit lines to data from 2 to 16 mA. Both sets of data indicate an intercept of 3.2Ω . This device has a $1\text{-}\mu\text{m}$ emitter width.

For a typical gain of $\beta = 50$, the term $(1 - \alpha_0)$ is around 0.02. C_{EX} is usually comparable in size or larger than C_{BC} and, thus, the capacitance ratio term will be between 0.5–1. For small devices, R_{B2} will typically be similar to the emitter resistance and, thus, the error on $r_e + R_E$ will be a few percent. The error is added to $r_e + R_E \Rightarrow r_e + R_E + \Delta R_{B2}$, which is then typically plotted versus the inverse emitter current in order to determine R_E (Fig. 9). That intercept is obtained by extrapolation to infinite emitter currents, and will also be shifted by the value of the correction term.

B. Effects of External Parasitics on Z -Parameter Method

The small-signal model used for the above derivations already includes the distributed base/collector effects, the output conductance effects, and the emitter contact resistance effect. The emitter inductance does not affect the real part of Z_{12} , and the base and collector external impedances are not part of Z_{12} . External pad capacitance effects should be small because the real part of Z_{12} should not be affected by a small external capacitance (i.e., the $(r_e + R_E)C_{pad}$ time constant is small). However, the dummy SHORT deembedding procedure is important. If the series resistances from the SHORT are deembedded in addition to series inductances, then the pad resistance will be directly removed from the extracted emitter resistance. Thus, inaccuracies in the SHORT add directly to the extracted emitter resistance.

C. From Y -Parameters

Another technique for the extraction of the emitter resistance is based on Y -parameters. When an impedance Z_E is added in series to the intrinsic hybrid- π model, shown in Fig. 2, then $1/Y_{21}$ becomes

$$\frac{1}{Y_{21}} = \frac{1 + Z_E g_m \left(1 - \frac{Z_E Y_{BE}}{1 + Z_E Y_{BE}}\right)}{g_m \left(1 - \frac{Z_E (Y_{BE} + Y_{BC})}{1 + Z_E Y_{BE}}\right)} - Y_{BC} \quad (38)$$

where $Y_{BE} = 1/r_\pi + j\omega C_\pi$ and $Y_{BC} = j\omega C_{BC}$ (neglecting the finite output impedance). At low frequencies, this reduces to

$$\frac{1}{Y_{21}} \approx \frac{1 + \frac{R_E}{r_\pi}}{g_m} + R_E = \frac{r_e + R_E}{\alpha}. \quad (39)$$

Since the hybrid- π model is identically equivalent to the T equivalent model, the above can be expressed in terms of the T equivalent parameters by using the relations in (6) as follows:

$$\frac{1}{Y_{21}} \approx \frac{r_e + R_E}{\alpha}. \quad (40)$$

Thus, when this quantity is plotted against the inverse emitter current (since $r_e = nkT/I_e$), the intercept with infinite emitter current will give the external emitter resistance times α_0 . Above dc, it may seem that the frequency dependences of $\alpha \sim \alpha_0(1 - j\omega\tau)$ and $j\omega C_\pi$ need be taken into account. However, the magnitude of $(1/Y_{21})$ will not change to first order since all the time constants in the above expression are typically much smaller than the measurement frequencies.

D. Effects of External Parasitics on the Y -Parameter Method

Of the external capacitances, only the input/output pad capacitance will affect the extracted resistance, but this capacitance is small compared with our device capacitances and can be neglected.

The emitter inductance will increase the apparent emitter resistance at high frequencies because of the decreased admittance Y_{21} . The effect of external impedances at the base and collector is somewhat more complicated. However, if the base/collector capacitance and output conductance are neglected, then it is readily shown that the collector impedance will not affect Y_{21} . The base impedance, on the other hand, will make $1/Y_{21}$ at low frequencies go to

$$\frac{1}{Y_{21}} \approx \frac{r_e + R_E}{\alpha} + R_B \left(\frac{1 - \alpha_0}{\alpha_0} \right). \quad (41)$$

Thus, the value of the intercept of $1/Y_{21}$ (i.e., the apparent external emitter resistance R_E) will increase with the external base resistance. In Fig. 9, emitter resistances extracted using both the Y - and Z -parameter methods are compared for $1\text{-}\mu\text{m}$ emitter width DHBTs. The absolute values of the apparent $r_e + R_E$ are clearly higher for the Y -parameter method data, and the intercepts (where r_e approaches zero) are 3.18 and 3.15Ω for the Y - and Z -parameter methods, respectively. The small difference appears consistent with a current gain of 80 (note that both Z -parameter methods include contributions from the base resistance). If accurate values of emitter resistance are required, then (41) can be used to calculate first-order correction terms. Additionally, the approximate external base resistance may be deembedded from measured S -parameters prior to emitter resistance calculation.

E. Current Gain Effects: Y - and Z -Parameter Methods

Since the current gain is not constant across the wide range of biases, another inaccuracy stems from the dependence of the extracted resistance on α . For our devices, the common emitter current gain may easily vary by a factor of four across the bias range used. Therefore, α_0 can easily vary by several percent. The term $1 - \alpha_0$ will vary by approximately the same factor as the current gain. Hence, in plots such as Fig. 9, the extracted emitter resistance does not form a straight line because of the lower gain at low currents. In order to compensate for such effects, multistep parameter-extraction procedures are required, first to determine the base resistance of a device, then to determine the current gain at each bias, and finally to calculate the total emitter resistance by either the Y - or Z -parameter methods.

VI. SUMMARY

Base/collector capacitance extraction for forward active biased HBTs using the Z -parameter method reliably gives the total intrinsic and extrinsic capacitance. Parasitic input/output capacitances directly add to the extracted base/collector capacitance, and parasitic output capacitances add a small term that is proportional to the common-base current gain. Finite output impedance is important only at low frequencies. Parasitic inductances at the collector increase the extracted capacitance. Base/collector capacitance extraction for "cold" HBTs should be performed using the Y -parameter method.

For base/emitter capacitance extraction, there is some difficulty in obtaining meaningful values of this capacitance because its first-order behavior can be accounted for by the transit time term τ in α . The extracted base/emitter capacitance includes a contribution from the transit time τ . Distributed base/collector effects do matter, more so for larger devices; very small devices can have base/emitter capacitances extracted more reliably across a wide range of frequencies. Finite output impedance does not affect the extracted base/emitter capacitance. Of the pad capacitances, only the input base pad capacitance is added to the extracted base/emitter capacitance.

In emitter resistance extraction using the Z -parameter method, the base resistance adds a correction term to the extracted emitter resistance. The error should be fairly small for high-speed HBTs. The estimated external emitter resistance R_E will be larger than the actual value by a few percent. In emitter resistance extraction using the Y -parameter method, the extracted total emitter resistance is too high by a factor of $1/\alpha$. Base resistances further add to the apparent external emitter resistance. For most accurate emitter resistance extraction using either method, the base resistance and current gain must also be determined.

ACKNOWLEDGMENT

The authors thank Dr. H. Rohdin, Agilent Technologies, Palo Alto, CA, for his corrections and suggestions.

REFERENCES

- [1] M. W. Dvorak, C. R. Bolognesi, O. J. Pitts, and S. P. Watkins, "Abrupt junction InP/GaAsSb/InP double heterojunction bipolar transistors with F_T as high as 250 GHz and $BV_{CEO} > 6$ V," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, 2000, pp. 178–181.
- [2] D. R. Pehlke and D. Pavlidis, "Evaluation of the factors determining HBT high-frequency performance by direct analysis of S -parameter data," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2367–2373, Dec. 1992.
- [3] S. J. Spiegel, D. Ritter, R. A. Hamm, A. Feygenson, and P. R. Smith, "Extraction of the InP/GaInAs heterojunction bipolar transistor small-signal equivalent circuit," *IEEE Trans. Electron Devices*, vol. 42, pp. 1059–1064, June 1995.
- [4] B. Li and S. Prasad, "Basic expressions and approximations in small-signal parameter extraction for HBT's," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 534–539, May 1999.
- [5] T.-S. Horng, J.-M. Wu, and H.-S. Huang, "An extrinsic-inductance independent approach for direct extraction of HBT intrinsic circuit parameters," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 2300–2305, Dec. 2001.
- [6] A. Ouslimani, J. Gaubert, H. Hafidallah, A. Birafane, P. Pouvil, and H. Leier, "Direct extraction of linear HBT-model parameters using nine analytical expression blocks," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 218–221, Jan. 2002.
- [7] S. Bousnina, P. Mandeville, A. B. Kouki, R. Surridge, and F. M. Ghanouchi, "Direct parameter-extraction method for HBT small-signal model," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 529–536, Feb. 2002.
- [8] A. P. Laser and D. L. Pulfrey, "Reconciliation of methods for estimating f_{MAX} for microwave heterojunction transistors," *IEEE Trans. Electron Devices*, vol. 38, pp. 1685–1692, Aug. 1991.
- [9] M. Vaidyanathan and D. L. Pulfrey, "Extrapolated f_{MAX} of heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 46, pp. 301–309, Feb. 1999.
- [10] C.-J. Wei and J. C. M. Hwang, "Direct extraction of equivalent circuit parameters for heterojunction bipolar transistors," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2035–2039, Sept. 1995.
- [11] P. J. van Wijnen, H. R. Claessen, and E. A. Wolsheimer, "A new straightforward calibration and correction procedure for "on-wafer" high frequency S -parameter measurements (45 MHz–18 GHz)," in *Proc. IEEE Bipolar Circuits and Technology Meeting*, Minneapolis, MN, 1987, pp. 70–73.
- [12] D. Peters, W. Daumann, W. Brockerhoff, R. Reuter, E. Koenig, and F. J. Tegude, "Direct calculation of the HBT small-signal equivalent circuit with special emphasize to the feedback capacitance," in *Eur. Microwave Conf. Dig.*, vol. 2, 1995, pp. 1032–1036.
- [13] M. Rudolph, R. Doerner, and P. Heymann, "Direct extraction of HBT equivalent-circuit elements," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 82–84, Jan. 1999.
- [14] C. Chang, P. Asbeck, P. Zampardi, and K. C. Wang, "Direct measurement of C_{bc} and C_{be} versus voltage for small HBT's with microwave S -parameters for scaled Gummel–Poon BJT models," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 108–110, Jan. 1999.



Martin W. Dvorak (S'97–M'03) was born in Toronto, ON, Canada, in 1973. He received the B.Sc. degree in engineering physics from Queen's University, Kingston, ON, Canada, in 1995, and the M.App.Sc. and Ph.D. degrees from Simon Fraser University, Burnaby, BC, Canada, in 1997 and 2002, respectively, both in engineering science. His doctoral dissertation involved the fabrication and characterization of ultra-high-speed InP/GaAsSb/InP DHBTs. These DHBTs were the first bipolar transistors to reach current gain cutoff frequencies in excess of 300 GHz.

Since 2001, he has been a Device Engineer with the Semiconductor Research and Development Division, Microwave Technology Center (MWTC), Agilent Technologies, Santa Rosa, CA, where he is involved in the development of MWTC's InP DHBT integrated circuit process.

Dr. Dvorak was the recipient of the International Electron Device (IEDM) 2000 Best Student Paper Award and the 2003 Natural Sciences and Engineering Research Council of Canada (NSERC) Doctoral Prize.



Colombo R. Bolognesi (S'84–M'94–SM'03) was born in St-Lambert, QC, Canada. He received the B.Eng. degree from McGill University, Montréal, QC, Canada, in 1987, the M.Eng. from Carleton University, Ottawa ON, Canada, in 1989, and the Ph.D. degree from the University of California at Santa Barbara, in 1994, all in electrical engineering. His Ph.D. dissertation focused on the physics and fabrication of InAs/AlSb-based HFETs.

He developed the first high-yield process for InAs/AlSb HFETs and, through innovations such as Te-delta doping and digital alloy Al(Sb,As) barrier engineering for HFETs, he demonstrated 0.5- μm devices with cutoff frequencies above 90 GHz. In 1994, he joined the Semiconductor Components Group, Northern Telecom, Ottawa, ON, Canada, as a BiCMOS Process Integration Engineer to develop a new generation of CMOS compatible 0.5- μm high-performance single-polysilicon emitter bipolar junction transistors (BJTs) with selectively implanted collectors. Among other topics, he has studied the effects of emitter fluorine incorporation and of emitter contact re-crystallization rate on device performance. In 1995, he joined Simon Fraser University (SFU), Burnaby, BC, Canada, as an Assistant Professor with a joint appointment between the School of Engineering Science and the Physics Department, to launch and direct SFU's Compound Semiconductor Device Fabrication Laboratory (CSDL). He became an Associate Professor in 1998 and a Professor in 2001. His current research interests focus on the development of millimeter-wave transistors [HBTs, high electron-mobility transistors (HEMTs)] and opto-electronic components based on new materials such as InP/GaAsSb, AlGaIn/GaN, and heterostructure device physics.

Dr. Bolognesi has served on the Technical Program and/or Executive Committees of several IEEE sponsored conferences such as the Device Research Conference (DRC'01 and DRC'02), the International Electron Device Meeting (IEDM'01–IEDM'03), and the Indium Phosphide and Related Materials Conference (IPRM'03). He has been the recipient of numerous prizes shared with students and collaborators, such as the IEEE 1999 GaAs IC Symposium Outstanding Paper Award and the 2001 New Frontiers in Research Award presented by the Science Council of British Columbia.